ABSTRACT

The widths of those portions of a semiconductor layer 5 and a drain line 6a overlapping with it which cross an edge line of a gate electrode 2 are made smaller than the channel width of a thin-film transistor. With this measure, the overlap area of the gate electrode 2 and a drain electrode 6 is reduced. As a result, a variation of the above overlap area due to alignment errors in a photolithography apparatus used in patterning the gate lines 2, the drain electrodes 6, and source electrodes 7 can be reduced and the frequency of occurrence of display defects can be decreased.